

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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IDS  
S. Davis  
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Applicant: Bulucea, Constantin  
Assignee: National Semiconductor Corporation  
Title: Gate-Enhanced Junction Varactor  
Application No.: 09/903,059 Filing Date: July 10, 2001  
Examiner: D. Farahani Group Art Unit: 2814  
Docket No.: NS-4971 US

San Jose, California  
June 13, 2002

COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR 1.97(c) WITH FEE**

Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the documents listed on the accompanying substitute PTO Form 1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

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Respectfully submitted,



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